WHAT IS CLAIMED IS:

1. A sense amplifier reference voltage generator circuit for nonvolatile memory devices, comprising:

at least one sense amplifier bias reference voltage generator (SABRVG) for generating a reference voltage at a reference node;

a start-up bias reference voltage generator (SBRVG) coupled to the SABRVG at the reference point;

a monitor reference voltage generator (MRVG) for generating a monitor reference voltage; and

a comparison module for comparing the monitor reference voltage with the reference voltage to produce a start-up control signal,

wherein the SBRVG enhances a discharging speed of the reference voltage during a reading cycle of the nonvolatile memory and when the monitor reference voltage and the reference voltage are matched, the start-up control signal stops the SBRVG from operating, thereby having the SABRVG maintain the reference voltage.

2. The circuit of claim 1 wherein the start-up bias reference voltage generator includes:

a pull-up pMOS transistor;

a first nMOS transistor for functioning as a reference memory cell with its gate controlled by a wordline control signal;

a second nMOS transistor connected in series with the first nMOS transistor with its gate controlled by a bitline control signal; and

a control module coupled between the pull-up pMOS transistor and the second nMOS transistor for turning on the SBRVG under a control of the start-up control signal.

3. The circuit of claim 2 wherein the control module further includes:

a third nMOS transistor with a negative feedback connected in series with the second nMOS transistor; and

a fourth nMOS transistor with its gate controlled by the start-up control signal and connected in series with the third nMOS transistor and the pull-up pMOS transistor.

4. The circuit of claim 1 wherein the SABRVG further includes:

a first and second pull-up pMOS transistors connected in parallel with a gate of the first pull-up pMOS transistor being controlled by a control signal and a drain of the second pull-up pMOS transistor generating the reference voltage;

a first nMOS transistor for functioning as a reference memory cell with its gate controlled by a wordline control signal;

a second nMOS transistor connected in series with the first nMOS transistor with its gate controlled by a bitline control signal; and

a third nMOS transistor with a negative feedback connected in series with the second nMOS transistor and the pull-up pMOS transistor,

wherein the reference voltage is coupled to one or more input/output modules of the nonvolatile memory.

5. The circuit of claim 4 wherein the comparison module has a current mirror type circuit for comparing the monitor reference voltage and the reference voltage and for producing the start-up control signal when enabled by the control signal.

6. The circuit of claim 1 wherein the MRVG further includes:

a first and second pull-up pMOS transistors connected in parallel with the gate of the first pull-up pMOS transistor being controlled by a control signal and the gate of the second pull-up pMOS transistor generating the monitor reference voltage;

a first nMOS transistor for functioning as a monitor memory cell with its gate controlled by a wordline control signal;

a second nMOS transistor connected in series with the first nMOS transistor with its gate controlled by a bitline control signal; and

a third nMOS transistor with a negative feedback connected in series with the second nMOS transistor and the pull-up pMOS transistors,

wherein the monitor reference voltage is not coupled to any input/output module of the nonvolatile memory.

7. The circuit of claim 1 wherein the SBRVG dissipates more current than the SABRVG at the beginning of the reading cycle.

8. A reference voltage generator circuit for nonvolatile memory devices, comprising:

at least one bias reference voltage generator (BRVG) for generating a reference voltage at a predetermined reference node thereof;

a start-up bias reference voltage generator (SBRVG) coupled to the reference node, the SBRVG further comprising:

a first pull-up pMOS transistor;

a first nMOS transistor for functioning as a reference memory cell with its gate controlled by a wordline control signal;

a second nMOS transistor connected in series with the first nMOS transistor with its gate controlled by a bitline control signal; and

a control module coupled between the first pull-up pMOS transistor and the second nMOS transistor for turning on the SBRVG under a control of a start-up control signal;

a monitor reference voltage generator (MRVG) for generating a monitor reference voltage; and

a comparison module for comparing the monitor reference voltage with the reference voltage to produce the start-up control signal,

wherein the SBRVG enhances a discharging speed of the reference voltage and when the monitor reference voltage and the reference voltage are matched, the start-up control signal stops the SBRVG from operating, thereby having the BRVG maintain the reference voltage.

9. The circuit of claim 8 wherein the BRVG further includes:

a second and third pull-up pMOS transistors connected in parallel with its gate of the second pull-up pMOS transistor being controlled by a control signal and its drain of the third pull-up pMOS transistor generating the reference voltage;

a third nMOS transistor for functioning as a reference memory cell with its gate controlled by a wordline control signal;

a fourth nMOS transistor connected in series with the third nMOS transistor with its gate controlled by a bitline control signal; and

a fifth nMOS transistor with a negative feedback connected in series with the fourth nMOS transistor and the pull-up pMOS transistors,

wherein the reference voltage is coupled to one or more input/output modules of the nonvolatile memory.

10. The circuit of claim 9 wherein the comparison module has a current mirror type circuit for comparing the monitor reference voltage and the reference voltage and for producing the start-up control signal when enabled by the control signal.

11. The circuit of claim 9 wherein the MRVG further includes:

a fourth and fifth pull-up pMOS transistors connected in parallel with the gate of the fourth pull-up pMOS transistor being controlled by the control signal and the gate of the fifth pull-up pMOS transistor generating the monitor reference voltage;

a sixth nMOS transistor for functioning as a monitor memory cell with its gate controlled by a wordline control signal;

a seventh nMOS transistor connected in series with the sixth nMOS transistor with its gate controlled by a bitline control signal; and

a eighth nMOS transistor with a negative feedback connected in series with the seventh nMOS transistor and the pull-up pMOS transistors,

wherein the monitor reference voltage is not coupled to any input/output module of the nonvolatile memory.

12. The circuit of claim 11 wherein the first pull-up pMOS transistor is a transistor larger than the similarly situated third and fifth pull-up pMOS transistors so that the SBRVG dissipates more current than the BRVG at the beginning of the reading cycle.

13. The circuit of claim 11 wherein the control module further includes:

a ninth nMOS transistor with a negative feedback connected in series with the second nMOS transistor; and

a tenth nMOS transistor with its gate controlled by the start-up control signal and connected in series with the ninth nMOS transistor and the pull-up pMOS transistors.

14. A method for enhancing reference voltage discharging speed during a reading cycle of a nonvolatile memory device, the method comprising:

generating a bias reference voltage at a reference point by at least one sense amplifier bias reference voltage generator (SABRVG);

enhancing the discharging speed of the bias reference voltage by coupling the reference point with a start-up bias reference voltage generator (SBRVG), the SBRVG further comprising:

a first pull-up pMOS transistor;

a first nMOS transistor for functioning as a reference memory cell with its gate controlled by a wordline control signal;

a second nMOS transistor connected in series with the first nMOS transistor with its gate controlled by a bitline control signal; and

a control module coupled between the first pull-up pMOS transistor and the second nMOS transistor for turning on the SBRVG under a control of a start-up control signal;

generating a monitor reference voltage by a monitor reference voltage generator (MRVG); and

comparing the monitor reference voltage with the reference voltage to produce the start-up control signal,

wherein when the monitor reference and the reference voltages are matched, the start-up control signal stops the SBRVG from operating, thereby having the SABRVG maintain the reference voltage.

15. The method of claim 14 wherein the SABRVG further includes:

a second and third pull-up pMOS transistors connected in parallel with the gate of the second pull-up pMOS transistor being controlled by a control signal and the gate of the third pull-up pMOS transistor generating the reference voltage;

a third nMOS transistor for functioning as a reference memory cell with its gate controlled by a wordline control signal;

a fourth nMOS transistor connected in series with the third nMOS transistor with its gate controlled by a bitline control signal; and

a fifth nMOS transistor with a negative feedback connected in series with the fourth nMOS transistor and the pull-up pMOS transistors,

wherein the reference voltage is coupled to one or more input/output modules of the nonvolatile memory.

16. The method of claim 14 wherein the MRVG further includes:

a fourth and fifth pull-up pMOS transistors connected in parallel with the gate of the fourth pull-up pMOS transistor being controlled by the control signal and the gate of the fifth pull-up pMOS transistor generating the monitor reference voltage;

a sixth nMOS transistor for functioning as a monitor memory cell with its gate controlled by a wordline control signal;

a seventh nMOS transistor connected in series with the sixth nMOS transistor with its gate controlled by a bitline control signal; and

an eighth nMOS transistor with a negative feedback connected in series with the seventh nMOS transistor and the pull-up pMOS transistors,

wherein the monitor reference voltage is not coupled to any input/output module of the nonvolatile memory.

17. The method of claim 16 wherein the first pull-up pMOS transistor is a transistor larger than the similarly situated third and fifth pull-up pMOS transistors so that the SBRVG dissipates more current than the SABRVG at the beginning of the reading cycle.